Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. OE**
2. **Q1**
3. **D1**
4. **D2**
5. **Q2**
6. **Q3**
7. **D3**
8. **D4**
9. **Q4**
10. **GND**
11. **LE**
12. **Q5**
13. **D5**
14. **D6**
15. **Q6**
16. **Q7**
17. **D7**
18. **D8**
19. **Q8**
20. **VCC**

**.057”**

**.061”**

**17 16 15 14**

**4 5 6 7**

**13**

**12**

**11**

**10**

**9**

**8**

**18**

**19**

**20**

**1**

**2**

**3**

**MASK**

**REF**

**25HCT373C**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Connect to Chip Back, Vcc or FLOAT**

**Mask Ref: 25HCT373C**

**APPROVED BY: DK DIE SIZE .057” X .061” DATE: 7/26/23**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 54HCT373**

**DG 10.1.2**

#### Rev B, 7/19/02